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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/653,788	09/01/2000	Stephen F. Smith	25016-49	5601

38396 7590 12/14/2004

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EXAMINER	
TRAN, KHAI	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/653,788	SMITH ET AL.
	Examiner	Art Unit
	KHAI TRAN	2637

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *24 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24,27,28 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6,8,15,16 and 19-24* is/are allowed.

6)☒ Claim(s) *1-5,7,9-14,17,18,27,28 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed 9/24/2004 has been entered. Claims 25-26, 29 have been cancelled. Claims 1-24, 27-28, and 30 are pending in this Office action.

Drawings

2. The drawings filed 9/24/2004 have been approved by Examiner.

Claim Objections

3. Claim 9 is objected to because of the following informalities: Appropriate correction is required.

Regarding claim 9, line 2, the term "signals" should be -- said signals--.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 9-12, 14, 17-18, 28, 30 are rejected under 35 U.S.C. 102(b) as being anticipated by DaSilva (U.S. Pat. 5,105,168).

Regarding claims 1, 2, 12, DaSilva discloses a digital data receiver synchronization apparatus as shown in Figure 3, comprising: a plurality of memory devices (a vector locked loops (10) having two phase locked loops (PLLs) (col. 3, lines 31-42)) for receiving multiple timing signals (64, 66) that are different in frequency, phase or both frequency and phase (i.e., when the loop is locked, the phase error and the magnitude error are driven to zero. The output signal will then track the phase,

frequency, and amplitude of the input signal (col. 3, lines 43-46), therefore the multiple timing signals are different in frequency, phase or both frequency and phase; feedback circuit (32, 36) interconnecting the memory devices and cross-coupling signals (48, 58) produced by the memory devices (PLLs in the vector locked loop 10); a common frequency reference source (i.e., comprising: VCO1 and VCO2 for driving the plurality of memory devices, see Figure 3, see col. 3, lines 9-46) in communication with the plurality of memory devices for driving the plurality of memory devices.

Regarding 3, DaSilva discloses wherein the multiple timing signals includes at least one signal selected from the group consisting of an RF carrier signal, a data bit-rate signal, a data chip-rate signal, a data frame-rate signal, and a data burst-or packet-rate signal (the vector locked loop is as a RF power amplifier (col. 6, lines 33-34), therefore, it is an FR carrier signal).

Regarding claims 4-5, DaSilva discloses that the vector locked loop (10) is somewhat similar to two cross-coupled phase locked loops, where both magnitude and phase are used as feedback signals (col. 3, lines 31-34) and DaSilva also discloses that the output signal will track the phase, frequency, and amplitude of the input signal. Therefore, the multiple timing signals are integrally or fractionally related in frequency, phase or both frequency and phase; and rationally multiply related in frequency and/or phase.

Regarding claim 9, DaSilva discloses wherein the signals cross-coupled by the feedback circuit include at least one member selected from the group consisting of error signals, and output signals (Figure 3 shows that error signal and output signal

generated by comparing the feedback signal with the input signal by using the phase detector 34).

Regarding claims 10-11, DaSilva discloses both magnitude and phase are used as feedback signals. Therefore, analog and digital signals are inherently included in the magnitude and phase signals.

Claims 14, 17 are similar to claims 1, and 9. Therefore, claims 14, 17 are rejected under a similar rationale.

Regarding claim 18, DaSilva also discloses the phase-frequency detector being a digital phase-frequency detector (Fig. 3).

Claim 28 is similar to claim 2. Therefore, claim 28 is rejected under a similar rationale.

Regarding claim 30, Dasilva also discloses at least one of the plurality of the memory devices includes a composite phase-frequency detector (the outputs of the phase and magnitude detectors used to track the phase, frequency of the input signal, see col. 3, lines 43-46).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7, 13, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over DaSilva (U.S. Pat. 5,105,168) in view of Lee (U.S. Pat. 5,568,078).

Regarding claim 7, DaSilva fails to disclose wherein the common frequency reference is an oscillator by a crystal, SAW device, ceramic resonator, mechanical resonator, dielectric resonator, or external source.

Lee discloses an oscillating output unit 1 as shown Fig. 2, for generating an external clock signal (as an external clock source). It would have been obvious to one having ordinary skill in the art at the time invention was made to utilize the external source for generating a reference frequency in order to enable the phase detector to compare the feedback signal with the reference frequency for reducing error rate.

Claim 13 is similar to claims 1 and 7. DaSilva also discloses the phase locked loop comprising phase-frequency detectors (34, 38). Therefore, claim 13 is rejected under a similar rationale.

Claim 27 is similar to claims 1 and 13. Therefore, claim 27 is rejected under a similar rationale.

Allowable Subject Matter

7. Claims 6,8 15-16, 19-24 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter: Dasilva and Lee fail to disclose or suggest that the multiple timing signals satisfy the relationship $f_1 = M \cdot f_2 = M \cdot N \cdot f_3$; wherein f_1 is RF signal; f_2 is said data bit rate signal; f_3 is said data frame-rate signal; and M and N are positive rational numbers.

Response to Arguments

9. Applicant's arguments filed 9/24/2004 have been fully considered but they are not persuasive.

Applicant states that in Dasilva the two VCOs are combined to produce the single composite output signal. In the claimed invention, the required VCOs have individual outputs (and at different frequencies).

In response to Applicant's argument that Dasilva disclose the two VCOs generating two different output signals 26 and 28.

Applicant states that the claimed invention is concerned with receiver synchronization, whereas Dasilva never even mentions the topic of synchronization.

In response to Applicant's argument that Dasilva discloses the feedback loop used in the phase locked loop (PLL). Dasilva did not mention a receiver synchronization. However; the use of a phase or frequency detector of the phase locked loop is for synchronizing frequency and phase between the digital reproduced signal and the reproducing clock signal.

Applicant states that Dasilva, both VCOs are each fed a single timing signal (16 and 18 respectively), whereas in the claimed invention, each VCO's operating frequencies is controlled by multiple (at least two) simultaneous timing signals developed from different sources.

In response to Applicant's argument that the limitation of each VCO's operating frequencies is controlled by multiple (at least two) simultaneous timing signals developed from different sources is not claimed.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHAI TRAN whose telephone number is (571) 272-3019. The examiner can normally be reached on 7:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JAY PATEL can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KHAI TRAN
Primary Examiner
Art Unit 2637

12/10/2004